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10/550,480	09/23/2005	Kyo-Seop Choo	ABS-2150 US	2994

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EXAMINER	
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2884	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,480	CHOO ET AL.	
	Examiner	Art Unit	
	Shun Lee	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

National Stage Application

Claim Objections

1. Claim 11 is objected to because of the following informalities:

(a) in claim 11, "forming a first transparent electrode on the first and second conductive lines; sequentially coating an insulating layer and an organic layer on the first transparent electrode" on lines 6-7 should probably be --forming first and second transparent electrodes on the first and second conductive lines, respectively; sequentially coating an insulating layer and an organic layer on the first and second transparent electrodes-- (since paragraph 54 of the specification discloses that referring " ... to FIG. 9, ITO materials 230 and 231 are deposited on the data pad region and the storage region of the resultant substrate as shown in FIG. 8, respectively ... "); and

(b) in claim 11, "forming a second transparent electrode for collecting electrons, the second transparent electrode being directly connected to the drain electrode and the first transparent electrode on the data pad, wherein the second transparent electrode over the second conductive line is formed on the insulating layer, thereby forming the storage capacitor between the second transparent electrode and the second conductive line" on lines 15-19 should probably be --forming third and fourth transparent electrodes for collecting electrons, the third transparent electrode being directly connected to the drain electrode and the fourth transparent electrode being directly connected to the first transparent electrode on the data pad, wherein the third transparent electrode over the second conductive line is formed on the insulating layer, thereby forming the storage

capacitor between the third transparent electrode and the second conductive line--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 11-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Amended independent claim 11 recites the limitation "forming a second transparent electrode for collecting electrons, the second transparent electrode being directly connected to the drain electrode and the first transparent electrode on the data pad, wherein the second transparent electrode over the second conductive line is formed on the insulating layer, thereby forming the storage capacitor between the second transparent electrode and the second conductive line".

However, the specification discloses (paragraph 59) that "Referring to FIG. 14, the ITO is deposited on a whole surface of the resultant substrate as shown in FIG. 13 for collecting electrons, and selectively etched away. Therefore, the ITO layer 260 is formed just on the data driver region, the data pad region, the TFT region and the storage capacitor region". The key phrase is "selectively etched away". Thus the selectively etched ITO layer 260 forms a third transparent electrode and

a fourth transparent electrode wherein the third transparent electrode is not directly connected the fourth transparent electrode (see Fig. 14). Therefore, the claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Claims 11-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification discloses (paragraph 25) that "When a scan signal for discharging the electrons from the storage capacitor C is transmitted from the gate driver 150 to the TFT, the TFT is turned on and the electrons are discharged through the drain and source electrode to the data pad 140". However (as discussed above), amended independent claim 11 requires the second transparent electrode to be directly connected to the drain electrode and the first transparent electrode on the data pad. However if the second transparent electrode is directly connected to both the drain electrode and the first transparent electrode on the data pad, the electrons are discharged to the data pad 140 even when the TFT is turned off. Therefore, the claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* (US 2001/0049154) in view of Kameshima (US 2002/0196898).

In regard to claims **4**, **6**, and **8**, Choo *et al.* disclose (Figs. 1-5) disclose an array panel comprising:

(a) a substrate (1, 171);

(b) a gate line (50, 150) extended on the substrate (1, 171) in a first direction;

(c) a data line (53, 153) extended on the substrate (1, 171) in a second direction;

(d) a switching element (T) including a gate electrode (73, 173), a source electrode (32, 132), and a drain electrode (33, 133), the switching element (T) being formed in a pixel region;

(e) a photoelectric cell (2) for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal;

(f) a pixel electrode (60, 62, 160, 211) formed in the pixel region, the pixel electrode (60, 62, 160, 211) comprises indium tin oxide ("ITO"; paragraphs 20 and 53) and gathering electrons generated from the photoelectric cell (2);

(g) an organic layer (83, 183; paragraphs 17 and 51) interposed between the pixel electrode (60, 62, 160, 211) and the switching element (T);

(h) a storage capacitor (S) formed in the pixel region, the storage capacitor (S) storing the electrons gathered by the pixel electrode (62, 211), wherein the storage capacitor (S) comprises a capacitor electrode (42, 142), a first transparent electrode (58, 158) formed directly on the capacitor electrode (42, 142), an insulating layer (15, 181), and the pixel electrode (60, 62, 160, 211) formed directly on the insulating layer (15, 181);

(i) a gate driver (*i.e.*, not shown "scanning integrated circuit"; paragraph 8) making an electrical contact with the gate line on the substrate (1, 171), the gate driver sequentially providing a scan signal for driving the switching element (T); and

(j) a data pad (paragraph 21) making an electrical contact with an end portion of the data line on the substrate (1, 171), the electrons stored in the storage capacitor (S)

being extracted to the data pad through the switching element (T) in case that the switching element (T) is turned on.

The panel of Choo *et al.* lacks an explicit description that the data pad makes an electrical contact with an end portion of the data line and the gate driver makes an electrical contact with an end portion of the gate line. Since Choo *et al.* do not disclose and/or require a specific scanning and/or data processing integrated circuitry location, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified circuitry location of Choo *et al.* as any one of the known conventional circuitry locations that did not require a detailed description. Further, Kameshima teaches (Figs. 7 and 8) that scanning and/or data processing integrated circuitry are located at the ends of the gate and data lines. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to locate the data pad and the gate driver at a known conventional location (*e.g.*, at the ends of the data and gate lines, respectively) in the panel of Kameshima.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Kameshima as applied to claim 4 above, and further in view of Jeon *et al.* (US 2002/0149318).

In regard to claim 5 which is dependent on claim 4, the modified panel of Choo *et al.* lacks that the gate driver includes a plurality of stages sequentially making an electrical contact with each other, each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each

stage being sequentially outputted from each output terminal, so that the stages function as a shift register. However, Choo *et al.* also disclose (paragraph 8) that the TFT "T" is turned ON by the scanning integrated circuit (not shown). Since Choo *et al.* do not disclose and/or require a specific scanning integrated circuit, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified scanning circuit of Choo *et al.* as any one of the known conventional scanning circuits that did not require a detailed description. Further, Jeon *et al.* teach a scanning circuit including shift register (164 in Fig. 5) comprising a plurality of stages sequentially making an electrical contact with each other, each of the stages including an input terminal, an output terminal (through which corresponding signals are transmitted), and a plurality of thin film transistors comprising amorphous silicon (paragraph 243) with a first clock signal and first control signal transmitted to odd numbered stages and second clock signal and second control signal transmitted to even numbered stages (paragraphs 109 and 110), a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, and wherein each of the stages includes: a pull-up driver (194 in Fig. 16) connected to an input node of a pull-up portion (190 in Fig. 16) that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal having a phase opposite (paragraph 109) to the phase of the first clock signal; a pull-down driver (196 in Fig. 16) connected to an input node of a pull-down portion (192 in Fig. 16) that applies a first voltage to the output terminal; the pull-up driver being turned on in accordance with the output signal of a previous stage, and

being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removed to remove the second clock signal; and the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to provide a known conventional scanning circuit (*e.g.*, comprising a plurality of stages, each including a pull-up driver connected to an input node of a pull-up portion and a pull-down driver connected to an input node of a pull-down portion) as the unspecified scanning circuit in the modified panel of Choo *et al.*

9. Claims 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Kameshima as applied to claim 4 above, and further in view of Jeromin *et al.* (US 6,075,248).

In regard to claim **7**, **9**, and **10** which are dependent on claim 4, the modified panel of Choo *et al.* lacks that the pixel electrode is disposed on a whole surface of the switching element and the gate driver with an organic layer interposed between the pixel electrode and the gate driver. However, Jeromin *et al.* teach (column 4, lines 21-24) to extend the electrode (18 in Fig. 1) over the FET (22 in Fig. 1). Further, Jeromin *et al.* teach to provide shielding electrodes (*e.g.*, 256 in Fig. 7) for circuitry, in order to minimize noise (column 4, line 64 to column 5, line 13). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to dispose the second transparent electrode on an insulating organic layer covering a

whole surface of the first and second switching element in the modified panel of Choo *et al.*, in order to minimize noise.

Response to Arguments

10. Applicant's arguments filed 17 February 2009 have been fully considered but they are not persuasive.

Applicant argues that the storage capacitor S as shown in Fig. 1 of Choo *et al.* has a first capacitor electrode 58 and an insulating dielectric layer 15 directly on the first capacitor electrode 58, without any structure that would correspond to the first transparent electrode. Examiner respectfully disagrees. Choo *et al.* disclose a storage capacitor (S in Fig. 1) comprising a capacitor electrode (42 in Fig. 1), a first transparent electrode (58 in Fig. 1) formed directly on the capacitor electrode (42 in Fig. 1), an insulating layer (15 in Fig. 1), and the pixel electrode (60, 62 in Fig. 1) formed directly on the insulating layer (15 in Fig. 1). Therefore, Choo *et al.* teach the capacitor structure as recited in amended independent claim 4.

Applicant argues that Kameshima, Jeon *et al.*, and/or Jeromin *et al.* fail to cure the deficiency in Choo *et al.* Examiner respectfully disagrees since Choo *et al.* teach the capacitor structure as recited in amended independent claim 4.

11. Applicant's arguments with respect to amended independent claim 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shun Lee whose telephone number is (571) 272-2439. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. L./
Examiner, Art Unit 2884

/David P. Porta/
Supervisory Patent Examiner, Art Unit 2884